ABSTRACT OF THE DISCLOSURE

The present invention of a storage control apparatus which is connected to a host bus connected to a CPU (Central Processing Unit), a peripheral bus connected to at least one IP (Intellectual Property), and a system memory and controls DMA (Direct Memory Access) transfer from the IP to the system memory, having: an address map judgment section which judges whether an address given from one of the peripheral bus and the host bus indicates a memory area managed by the storage control apparatus in the system memory; a memory control section which controls data transfer to/from the system memory; a TLB (Translation Look-aside Buffer) information holding section which holds address information that indicates an area cacheable by the CPU; an address judgment section which judges on the basis of the address information held by the TLB information holding section whether the address given from one of the peripheral bus and the host bus indicates the area cacheable by the CPU; and a snoop address control section which, when it is judged on the basis of a judgment result from the address judgment section that the CPU needs to be notified of the address, executes notification through the host bus.